Introduction

• Goal of our research:

• Improve the productivity & performance of applications on distributed-memory machines

• Our central idea: shared memory + task parallelism

• Two general programming models applicable to arbitrary parallel computation patterns • Intuitive global-view programming

- Distributed Shared Memory (DSM) • Physically distributed, virtually shared
- The system automatically synchronizes the caches between cores



History of DSM

- 1990s: Early DSM systems appeared
- e.g. TreadMarks [Keleher et al. '94], JIAJIA [Hu et al. '98]
- 2000s-: **PGAS** systems replaced them
- e.g. UPC [El-Ghazawi et al. '02], Global Arrays [Nieplocha et al. '06], OpenSHMEM [Chapman et al. '10]
- Scalable & global-view programming models
- Explicit communications are still burdensome

• Why DSM again?

- Improvement of network speed [Ramesh '13]
- Inter-node latency / DRAM latency $\approx 1000 (1990s)$, 10 times (2010s)
- Inter-node bandwidth / DRAM bandwidth ≈ 500 (1990s), 2.5 times (2010s)
- **2** Relationship with **many-core** architectures
- Shared memory is considered as a bottleneck of scalability
- Techniques for software DSMs are revisited

Cache invalidation methods

- Directory-based coherence
- The state-of-the-art method to implement large-scale shared memory • Tracking sharers in centralized directories



• Problems of directories: O(P) storage cost to hold sharers (*P*: # of nodes) **2** Communication traffic of small invalidation messages **3** Complex state management leads to system bugs

• Logical-timestamp-based coherence [Yu et al. '15] • Invalidate cache blocks based on logical timestamps (= Lamport clocks)



- Pros of logical-timestamp-based coherence • Only $O(\log P)$ storage is required
- No explicit invalidation message is needed
- Cons of logical-timestamp-based coherence
- Unnecessary cache invalidations (= cache misses) due to the nature of logical timestamps



A Distributed Shared Memory Library with Global-View Tasks on High-Performance Interconnects Wataru Endo, Kenjiro Taura (Graduate School of Information Science and Technology, The University of Tokyo)



• Ongoing efforts for performance improvements • e.g. multi-threading communication performance, prefetching

- one of them has benchmark threads repeating RDMA READ

CPU	Intel [®] Xeon [®] E5-2680 v2
	2.80GHz, 2 sockets× 10 cores/node
Memory	16GB/node
nterconnect	Mellanox [®] Connect-IB [®] dual port
	InfiniBand FDR 2-port (only 1 port is used)
Driver	Mellanox [®] OFED 2.4-1.0.4
DS	Red Hat [®] Enterprise Linux [®] Server
	release 6.5 (Santiago)
Compiler	GCC 4.4.7 (with the option "-O3")

- Used MassiveThreads 0.97 for user-level threading • Change to use parent-first scheduling (child-first is the default)
- Run only 10 worker threads/node to avoid NUMA effects
- Compare 3 different methods:







- architectures • Future work
- Analyze the bottlenecks of the DSM
- Reduce the latency of software offloading

References